MN8601

High-performance CMOS Digital Signal Processor (DSP)

■ Outline

The MN8601 is a high-performance CMOS digital signal processor with 16-bit data accuracy which has functions required for digital signal processing.
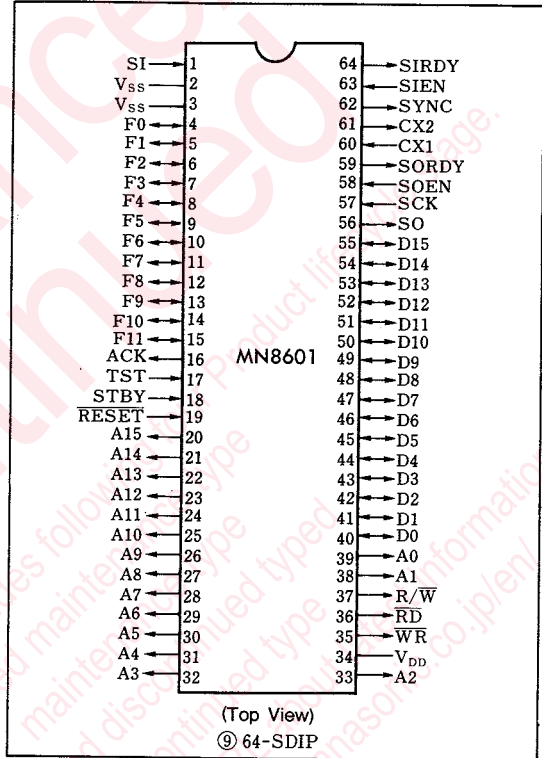It incorporates a pair of large-capacity data RAMs and an instruction ROM.

A signal processing procedure can be flexibly programmed by an 8-bit(word length)macro-instruction or 32-bit micro-instruction to allow various system configurations and a wide range of application.
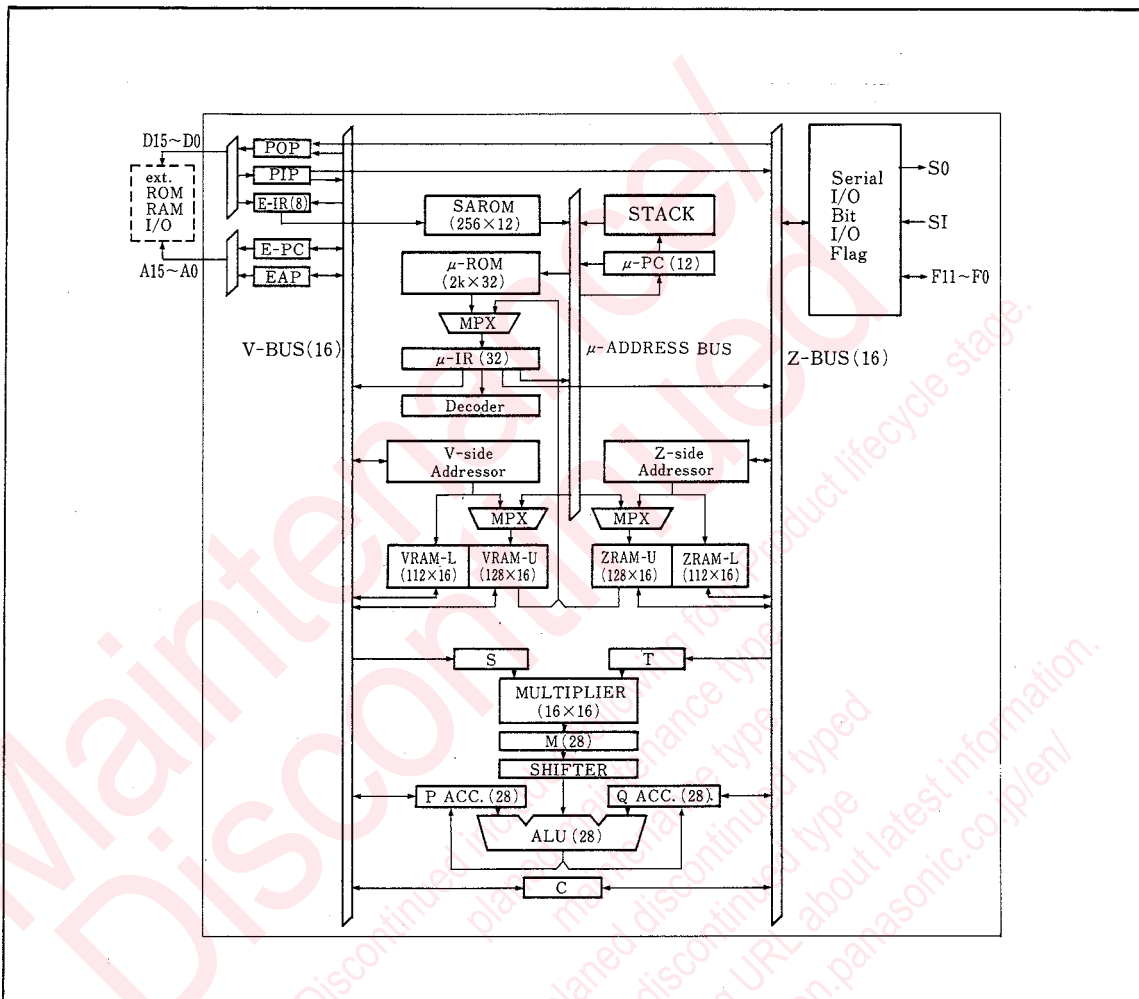
■ Featrues

● High-speed operation:Machine cycle 190 ns
● Large-capacity built-in RAM:240 words x 16 bits
  x 2
● Built-in instruction ROM:2,048 words x 32 bits
● Built-in parallel multiplier:16 bits→28 bits
● Internal RAM configuration variable architecture:
  Internal RAM switchable as data RAM or micpropro-
  gram RAM.
● ALU accumalator:28 bits
● Basic data accuracy:16 bits
  high-accuracy operation enabled
● Interface
  64K-word external memory space
  16-bit data bus
  Serial interface
  12-bit I/O ports
● Software
  Flexible programming by marco-instruction sets
  and micro-instruction sets
  8-bit vertical macro-instructions
  32-bit horizontal macro-instructions
● CMOS 5 V single power supply
● 64-pin shrunk DIP plastic package
  (64-SDIP)

■ Pin Configuration

Pin	Signal	Pin	Signal
1	SI	64	SIRDY
2	Vss	63	SIEN
3	Vss	62	SYNC
4	F0	61	CX2
5	F1	60	CX1
6	F2	59	SORDY
7	F3	58	SOEN
8	F4	57	SCK
9	F5	56	SO
10	F6	55	D15
11	F7	54	D14
12	F8	53	D13
13	F9	52	D12
14	F10	51	D11
15	F11	50	D10
16	ACK	49	D9
17	TST	48	D8
18	STBY	47	D7
19	RESET	46	D6
20	A15	45	D5
21	A14	44	D4
22	A13	43	D3
23	A12	42	D2
24	A11	41	D1
25	A10	40	D0
26	A9	39	A0
27	A8	38	A1
28	A7	37	R/W
29	A6	36	RD
30	A5	35	WR
31	A4	34	VDD
32	A3	33	A2

MN8601

(Top View)
⑨ 64-SDIP

■ Block Diagram

■ Absolute Maximum Ratings (V$_{SS}$=0V, T$_a$=25°C)

Item	Symbol	Rating	Unit
Suply voltage	V$_{DD}$	$-0.3 \sim +7.0$	V
Input voltage	V$_{IN}$	$-0.3 \sim +7.0$	V
Output pin voltage	V$_o$	$-0.3 \sim +7.0$	V
I/O pin voltage	V$_{IO}$	$-0.3 \sim +7.0$	V
Operating ambient temperature	T$_{opr}$	$0 \sim +70$	°C
Storage temperature	T$_{stg}$	$-55 \sim +125$	°C

■ Operating Conditions

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply voltage	V$_{DD}$	t$_c \geqq$190ns	4.75	5.00	5.25	V
Execution time	t$_c$		190		4000	ns
Clock frequency	f$_{cp}$		1.00		21.0526	MHz

■ Electrical Characteristics ($V_{SS}=0V$, $V_{DD}=4.75$ to $5.25V$, $f=21.0526MHz$)

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply current	I_{DD}	$f_{CP}=21.0526MHz$		20	50	mA
Input voltage high level (Clock pin)	V_{IHOSC}		$0.8V_{DD}$		V_{DD}	V
Input voltage low level (Clock pin)	V_{ILOSC}		V_{SS}		0.5	V
Input voltage high level (Other than clock pin)	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage low level (0ther than clock pin)	V_{IL}		V_{SS}		0.8	V
Input current (W/O pull-up)	I_I				±10	μA
Input current (W/ pull-up)	I_{IVR}	$V_{IN}=0.8V$			-300	μA
Output voltage high level	V_{OH}	$I_{OH}=-400\mu A$	$V_{DD}-0.4$		V_{DD}	V
Output voltage low level	V_{OL}	$I_{OL}=1.6mA$	V_{SS}		0.4	V
Bus cycle time	t_{CYC}		380		8000	ns
Read/write pulse width (High)	t_{RWWH}		320			ns
Read/write pulse width (Low)	t_{RWWR}		320			ns
Address delay time	t_{AD}				40	ns
Address hold time (At read time)	t_{AHR}		0			ns
Address hold time (At write time)	t_{AHW}		15			ns
Read/write hold time (At write time)	t_{RWHW}	$V_{DD}=5.0$, $V_{SS}=0V$ $V_{IH}=0.7V_{DD}$, $V_{IL}=0.8V$ $V_{OH}=0.7V_{DD}$, $V_{OL}=0.8V$	15			ns
Read pulse width	t_{RDW}		130			ns
Write pulse width	t_{WRW}		90			ns
Peripheral read access time	t_{ACC}				250	ns
Data setup time (At read time)	t_{DSR}		70			ns
Data setup time (At write time)	t_{DSW}		120			ns
Data hold time (At read time)	t_{DHR}		10			ns
Data hold time (At write time)	t_{DHW}		15			ns
Clock cycle time	t_{CP}	$V_{DD}=5.0$, $V_{SS}=0V$ $V_{IH}=0.8V_{DD}$, $V_{IL}=0.5V$	47.5			ns
Clock high level pulse width	t_{WCPH}		15			ns
Clock low level pulse width	t_{WCPL}		15			ns

■ Pin Descriptions

| Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	SI	Serial Input	33	A2	Address BUS2
2	V$_{SS}$	V$_{SS}$ Power Supply	34	V$_{DD}$	V$_{DD}$ Power Supply
3	V$_{SS}$	V$_{SS}$ Power Supply	35	$\overline{WR}$	Write pulse
4	F0	General Flag0	36	$\overline{RD}$	Read pulse
5	F1	General Flag1	37	R/$\overline{W}$	Read/Write
6	F2	General Flag2	38	A1	Address BUS1
7	F3	General Flag3	39	A0	Address BUS0
8	F4	General Flag4	40	D0	Data BUS0
9	F5	General Flag5	41	D1	Data BUS1
10	F6	General Flag6	42	D2	Data BUS2
11	F7	General Flag7	43	D3	Data BUS3
12	F8	General Flag8	44	D4	Data BUS4
13	F9	General Flag9	45	D5	Data BUS5
14	F10	General Flag10	46	D6	Data BUS6
15	F11	General Flag11	47	D7	Data BUS7
16	ACK	Acknowledge	48	D8	Data BUS8
17	TST	Test	49	D9	Data BUS9
18	STBY	Stand by	50	D10	Data BUS10
19	$\overline{RESET}$	Reset	51	D11	Data BUS11
20	A15	Address BUS15	52	D12	Data BUS12
21	A14	Address BUS14	53	D13	Data BUS13
22	A13	Address BUS13	54	D14	Data BUS14
23	A12	Address BUS12	55	D15	Data BUS15
24	A11	Address BUS11	56	SO	Serial Output
25	A10	Address BUS10	57	SCK	Serial Clock
26	A9	Address BUS9	58	SOEN	Serial Out Enable
27	A8	Address BUS8	59	SORDY	Serial Out Ready
28	A7	Address BUS7	60	CX1	Cristal 1
29	A6	Address BUS6	61	CX2	Cristal 2
30	A5	Address BUS5	62	SYNC	SYNC
31	A4	Address BUS4	63	SIEN	Serial Input Enable
32	A3	Address BUS3	64	SIRDY	Serial Input Ready

■ Timing Diagrams

● Read Timing
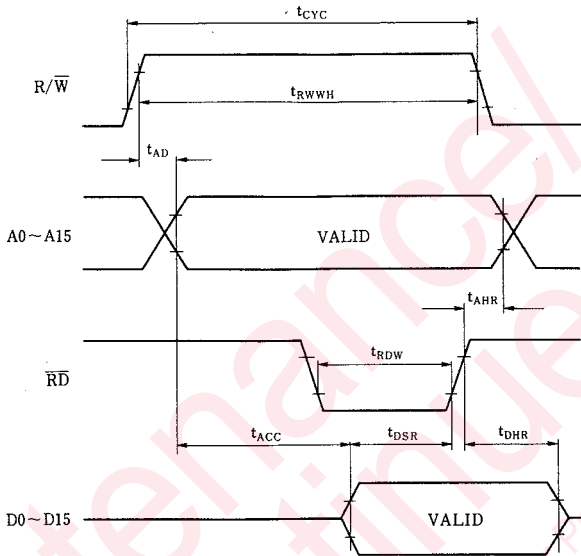
● Write Timing
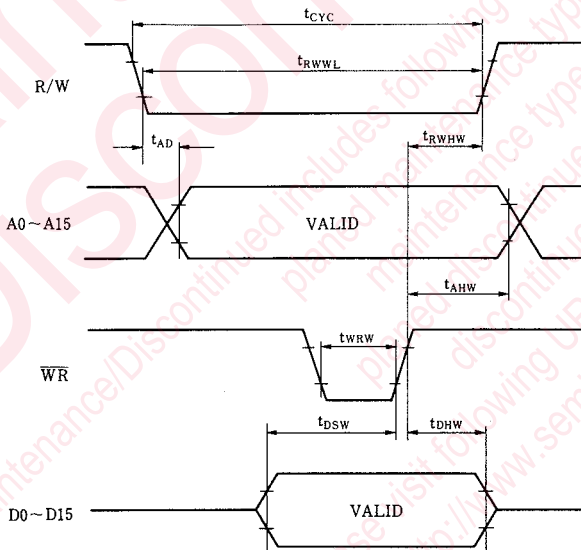
● Clock Waveform
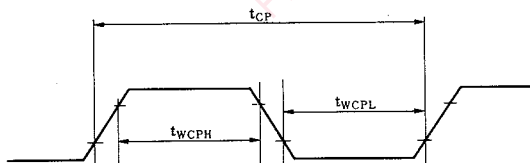
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